



1/8

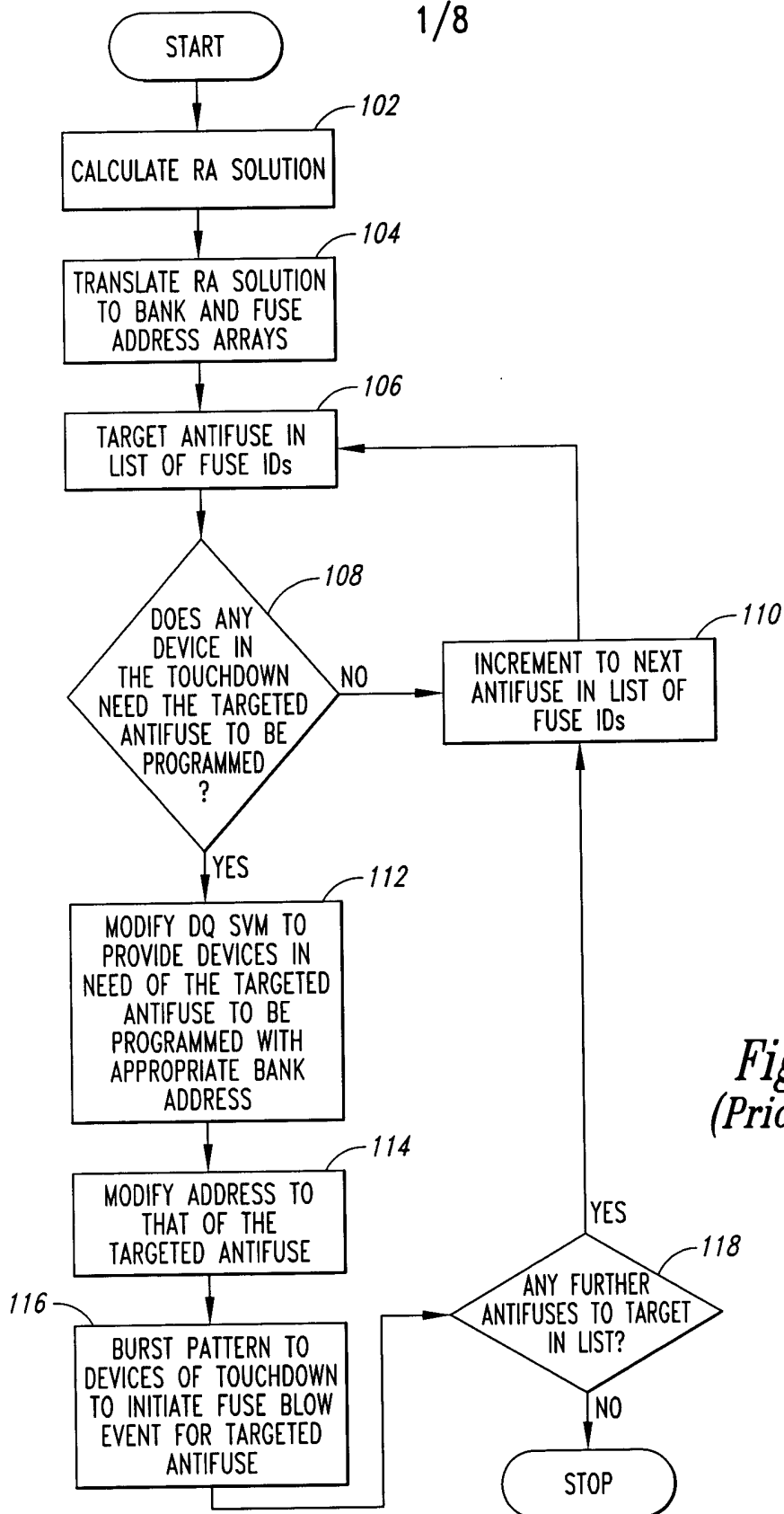


Fig. 1
(Prior Art)

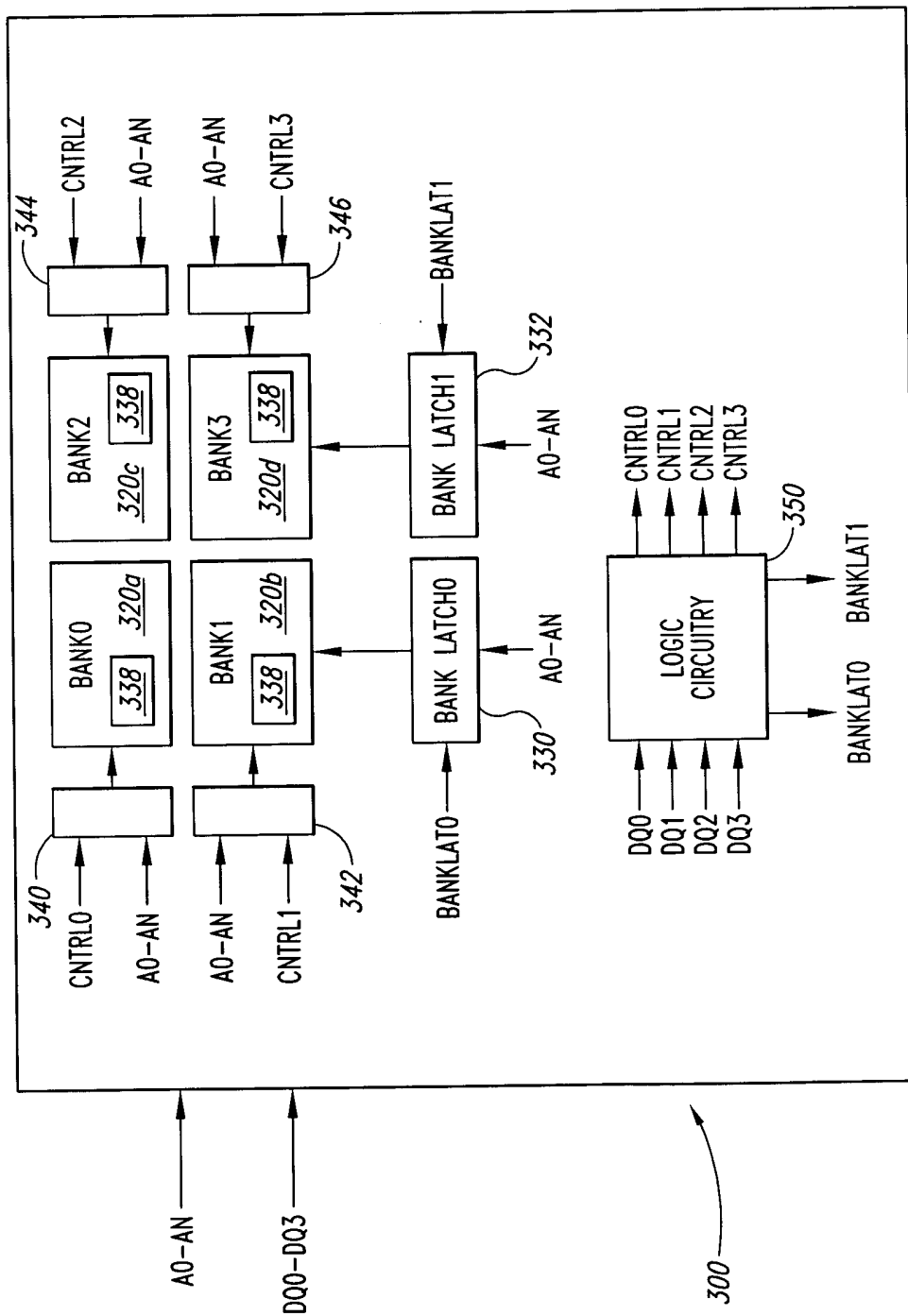


Fig. 2

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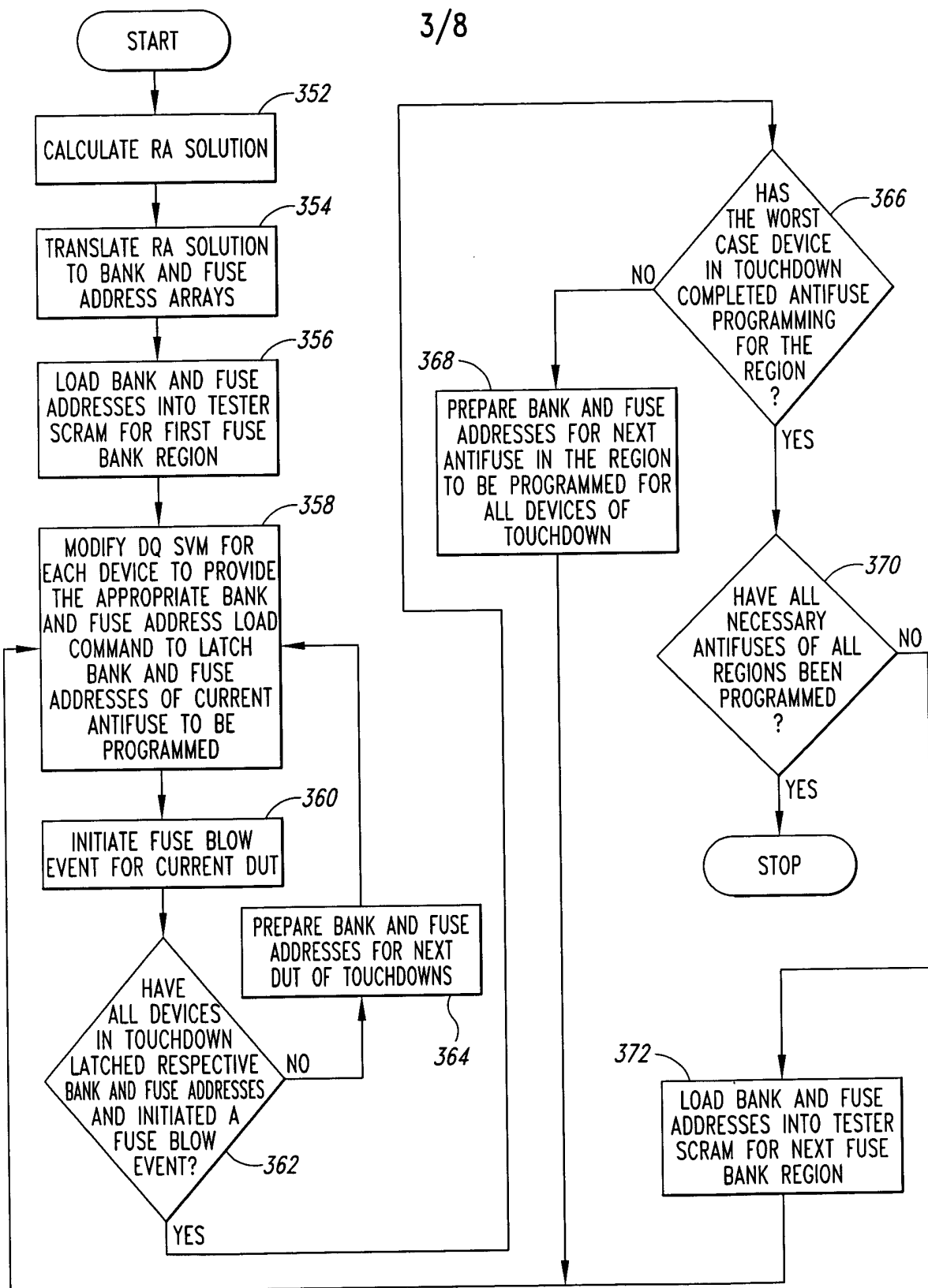


Fig. 3



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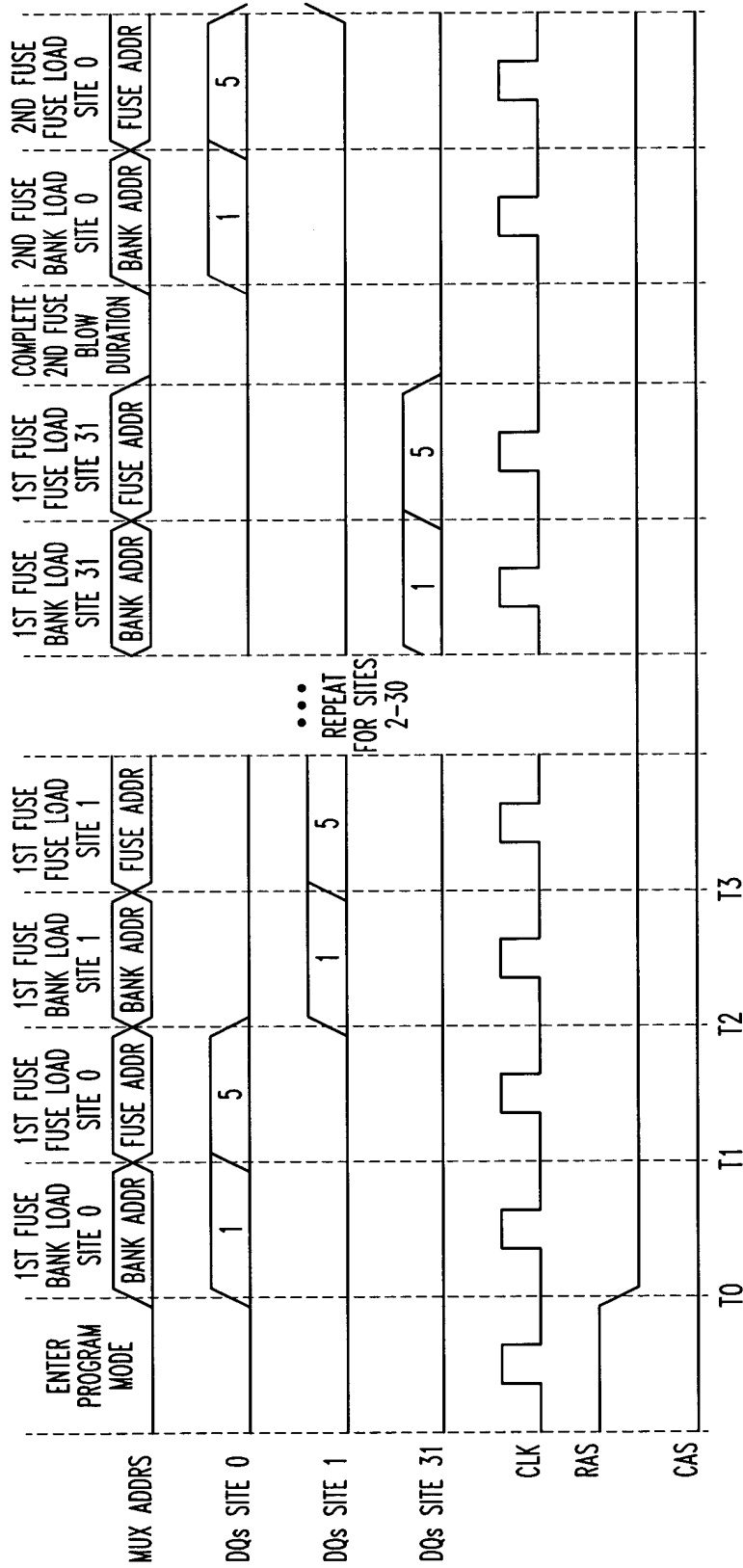


Fig. 4



500

SCRAM RAM		DQ SVM DATA					
		DUT 0	DUT 1	...	DUT 31	...	DUT 63
		0123	0123	...	0123	...	0123
502	BANK	1000	0000	...	0000	...	0000
504	FUSE	1010	0000	...	0000	...	0000
502	BANK	0000	1000	...	0000	...	0000
504	FUSE	0000	1010	...	0000	...	0000
...							
502	BANK	0000	0000	...	1000	...	0000
504	FUSE	0000	0000	...	1010	...	0000
...							
502	BANK	0000	0000	...	0000	...	1000
504	FUSE	0000	0000	...	0000	...	1010

Fig. 5



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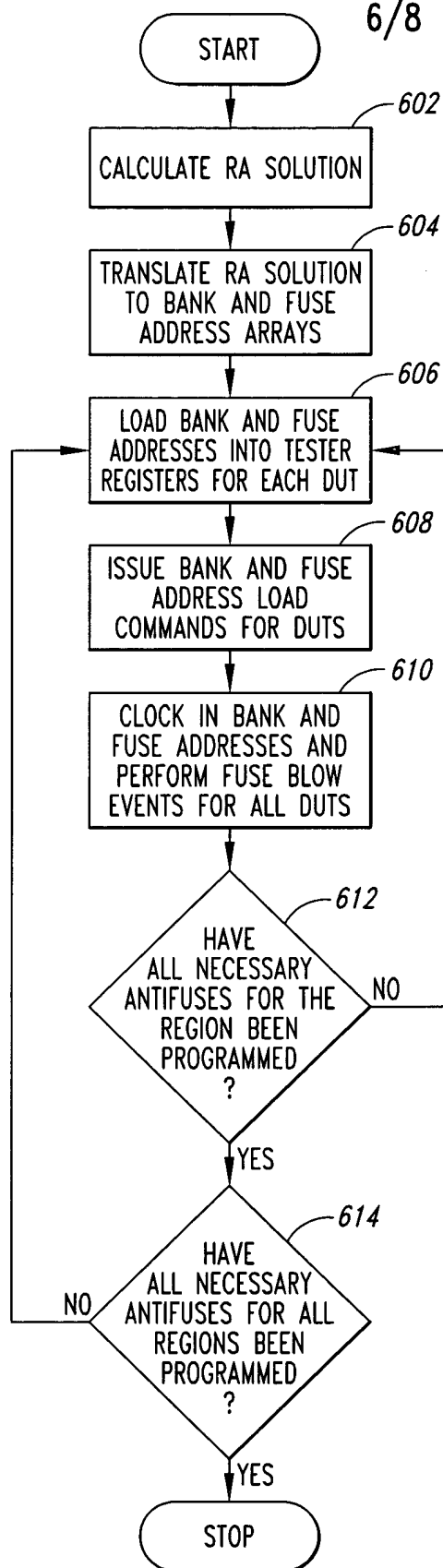


Fig. 6





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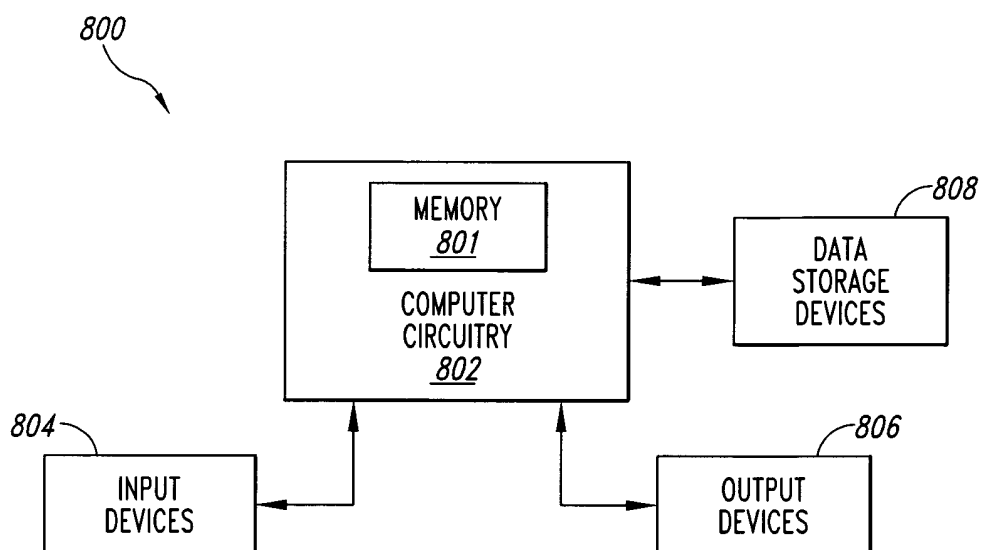


Fig. 8